

**IN THE SPECIFICATION:**

**Paragraph beginning at line 22 of page 2 has been amended as follows:**

In general, as shown in Fig. 6, the output of the output circuit that constitutes the inverter becomes ~~ineonstant~~ unstable at a voltage equal to or lower than its operation voltage. This is because both of the p-ch MOS Tr 18 and n-ch MOS Tr 19 which constitute the output circuit 20 are enhancement-type transistors, and therefore the transistors cannot be turned on unless a voltage equal to or higher than a threshold voltage of the transistors is applied between the gate and source of the transistors.

**Paragraph beginning at line 6 of page 3 has been amended as follows:**

That is, because both of the p-ch MOS Tr 18 and the n-ch MOS Tr 19 are in an off-state at the voltage equal to or lower than the threshold voltage of the transistors, the voltage of the output terminal 12 becomes unstable ~~ineonstant~~.

**Paragraph beginning at line 13 of page 4 has been amended as follows:**

In order to achieve the above object, according to the present invention, a ~~depression-type~~ depletion-type MOS

transistor is added to an output terminal of a voltage detecting circuit so as to provide an accurate voltage detection output even if the voltage detecting circuit is at or below an operation voltage of the transistor ~~or lower~~.

**Paragraph beginning at line 12 of page 5 has been amended as follows:**

In the voltage detecting circuit according to the present invention, the second output circuit includes a ~~depression-type~~ depletion-type n-ch MOS transistor and ~~depression-type~~ depletion-type p-ch MOS transistor which are connected in series between the output terminal and one of the first terminal and the second terminal. Further, in the voltage detecting circuit according to the present invention, a signal based on a voltage of the first terminal is input ~~inputted~~ to a gate electrode of the ~~depression-type~~ depletion-type p-ch MOS transistor, and a signal based on a voltage of the second terminal is inputted to a gate electrode of the ~~depression-type~~ depletion-type n-ch MOS transistor.

**Paragraph beginning at line 22 of page 5 has been amended as follows:**

In the voltage detecting circuit according to the present invention, the first output circuit includes an enhancement-type n-ch MOS transistor and an enhancement-type

p-ch MOS transistor which are connected in series between the first terminal and the second terminal. Further, in the voltage detecting circuit according to the present invention, a signal based on the output of the comparator is inputted to gate electrodes of the enhancement-type p-ch MOS transistor and the enhancement-type n-ch MOS transistor. Still further, in the voltage detecting circuit according to the present invention, an absolute value of any threshold voltages ~~voltage~~ of the ~~depression-type~~ depletion-type n-ch MOS transistor and the ~~depression-type~~ depletion-type p-ch MOS transistor is larger than an absolute value of any threshold voltages ~~voltage~~ of the enhancement-type n-ch MOS transistor and the enhancement-type p-ch MOS transistor.

**Paragraph beginning at line 13 of page 7 has been amended as follows:**

Fig. 1 is a diagram showing a voltage detecting circuit in accordance with a first embodiment of the present invention. A difference between Figs. 1 and 6 resides in that a ~~depression-type~~ depletion-type n-ch MOS Tr 21 and a ~~depression-type~~ depletion-type p-ch MOS Tr 22 are connected to an output terminal 12. The basic voltage detecting operations are the same as those in the conventional voltage detecting circuit.

Paragraph beginning at line 19 of page 7 has been amended as follows:

When a voltage  $V_1$  across a battery 1 is lower than threshold voltages of enhancement-type MOS Tr 18 and 19, both of the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 turn on with the result that the output of the output terminal 12 becomes L in level.

Paragraph beginning at line 1 of page 8 has been amended as follows:

In this example, when an absolute value of the threshold value of the ~~depression-type~~ depletion-type p-ch MOS Tr 22 is made equal to or slightly larger than an absolute value of the threshold value of the enhancement-type n-ch MOS Tr 19, the enhancement-type n-ch MOS Tr 19 can turn on before the voltage across the battery  $V_1$  at which the ~~depression-type~~ depletion-type p-ch MOS Tr 22 turns off is reached, whereby the voltage level of the output terminal 12 can be kept to L.

Paragraph beginning at line 8 of page 8 has been amended as follows:

In addition, when the voltage  $V_1$  across the battery 1 is ~~stepped-up~~ increased, the ~~depression-type~~ depletion-type

p-ch MOS Tr 22 turns off in a short time, and a path through which the output terminal 12 is lowered to L by the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 becomes high in impedance and does not function. In this state, the voltage detecting circuit according to the present invention is equivalent to the conventional voltage detecting circuit.

**Paragraph beginning at line 16 of page 8 has been amended as follows:**

When the voltage V1 of the battery 1 is further increased ~~stepped up~~, the voltage V1 becomes the detected voltage of the voltage detecting circuit in a short time, and the voltage of the output terminal 12 is changed from L level to H level at that voltage.

**Paragraph beginning at line 20 of page 8 has been amended as follows:**

After changing to the H level, since the ~~depression-type~~ depletion-type n-ch MOS Tr 21 turns off, the voltage detecting circuit according to the present invention is equivalent to the conventional voltage detecting circuit.

Paragraph beginning at line 24 of page 8 ha been amended as follows:

Fig. 2 shows a voltage V12 of the output terminal 12 in an ordinate axis when the voltage V1 across the battery 1 of the voltage detecting circuit according to the present invention is changed as an abscissa axis. In a region B of Fig. 2, since both of the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr22 are on, the voltage at the output terminal 12 is maintained at an L level.

Paragraph beginning at line 7 of page 9 has been amended as follows:

In other words, the voltage detecting circuit according to the present invention eliminates an ~~inconstant~~ unstable region (uncertain output region) of the voltage detecting circuit at the time of a low voltage without increasing a consumed current of the voltage detecting circuit, and conducts the same operation as that of the conventional voltage detecting circuit when the voltage is high.

Paragraph beginning at line 13 of page 9 has been amended as follows:

Fig. 3 shows a voltage detecting circuit in accordance with a second embodiment of the present invention. Differences of Fig. 3 from Fig. 1 reside in that the inverter circuit 17 is removed, the output of the comparator 16 is connected to the input of the output circuit 20, and electric elements connected in series to the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 are connected between the output terminal 12 and the terminal 11, that is, to the plus side of the battery 1.

Paragraph beginning at line 21 of page 9 has been amended as follows:

In addition, in Fig. 3, since there is no ~~provision~~ ~~of the inverter 17~~, the L level and H level of the output terminal 12 are inverted with respect to the voltage across the battery 1 as compared with the case of Fig. 1. That is, the output terminal 12 becomes H in level when the voltage across the battery 1 is the detected voltage or lower, whereas the output terminal 12 becomes L in level when the voltage across the battery 1 is the detected voltage or higher.

Paragraph beginning at line 4 of page 10 has been amended as follows:

When a voltage V1 across a battery 1 is lower than threshold voltages of enhancement-type MOS Tr 18 and 19, both of the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 turn on with the result that the output of the output terminal 12 becomes H in level.

Paragraph beginning at line 9 of page 10 has been amended as follows:

In this example, when an absolute value of the threshold value of the ~~depression-type~~ depletion-type n-ch MOS tr 21 is made equal to or slightly larger than an absolute value of the threshold value of the enhancement-type p-ch MOS Tr 18, the enhancement-type p-ch MOS Tr 18 can turn on before the voltage across the battery V1 at which the ~~depression-type~~ depletion-type n-ch MOS Tr 21 turns off, whereby the voltage level of the output terminal 12 can be kept to H.

Paragraph beginning at line 16 of page 10 has been amended as follows:

In addition, when the voltage V1 across the battery 1 is ~~stepped up~~ increased, the ~~depression-type~~ depletion-type

n-ch MOS Tr 21 turns off in a short time, and a path through which the output terminal 12 is raised to H by the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 becomes high in impedance and does not function. In this state, the voltage detecting circuit according to the present invention is equivalent to the conventional voltage detecting circuit.

**Paragraph beginning at line 24 of page 10 has been amended as follows:**

When the voltage V1 of the battery 1 is further increased ~~stepped-up~~, the voltage V1 becomes the detected voltage of the voltage detecting circuit in a short time, and the voltage of the output terminal 12 is changed from H level to L level at that voltage.

**Paragraph beginning at line 4 of page 11 has been amended as follows:**

After changing to L level, since the ~~depression-type~~ depletion-type p-ch MOS Tr 22 turns off, the voltage detecting circuit according to the present invention is equivalent to the conventional voltage detecting circuit.

Paragraph beginning at line 8 of page 11 has been amended as follows:

Fig. 4 shows a voltage V12 of the output terminal 12 in an ordinate axis when the voltage V1 across the battery 1 of the voltage detecting circuit according to the present invention is changed as an abscissa axis. In a region B of Fig. 4, since both of the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22 are on, the voltage at the output terminal 12 is maintained H in level.

Paragraph beginning at line 21 of page 11 has been amended as follows:

Fig. 5 is a diagram shown a voltage detecting circuit in accordance with a third embodiment of the present invention. A difference between Figs. 1 and 5 resides in that a ~~depression-type~~ depletion-type n-ch MOS Tr 31 and a ~~depression-type~~ depletion-type p-ch MOS Tr 32 are connected to the output of the comparator 16.

Paragraph beginning at line 11 of page 12 has been amended as follows:

However, because the output terminal 12 is connected with the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the

~~depression-type~~ depletion-type p-ch MOS Tr 22, the output terminal 12 is lowered to L level, and a path that is rendered conductive between the terminals 11 and 10 is generated by the enhancement-type p-ch MOS transistor 18, the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the ~~depression-type~~ depletion-type p-ch MOS Tr 22, thereby allowing an ineffective current to flow. Similarly, because the output voltage at the terminal 12 is determined in accordance with the on-resistance of the enhancement-type p-ch MOS Tr 18, the on-resistance of the ~~depression-type~~ depletion-type n-ch MOS Tr 21 and the on-resistance of the ~~depression-type~~ depletion-type p-ch MOS Tr 22, an L level cannot be maintained. As its countermeasure, the ~~depression-type~~ depletion-type n-ch MOS Tr 31 and the ~~depression-type~~ depletion-type p-ch MOS Tr 32 are added to the output of the comparator 16, and the output of the comparator 16 is determined to be L in level at the time of the operation voltage of the comparator 16 or lower, thereby being capable of surely bringing the output terminal 12 into L level when the voltage of the battery 1 is low.

**Paragraph beginning at line 5 of page 13 has been amended as follows:**

As described above, according to the present invention, the ~~ineonstant~~ unstable region when the voltage detecting circuit operates at a low voltage can be eliminated.

Paragraph beginning at line 8 of page 13 has been amended as follows:

As was described above, according to the present invention, there is an effect in that since the ~~inconstant~~ unstable region at the time of the low voltage is eliminated without increasing the consumed current, malfunction due to an error voltage detection signal (for example, a reset signal to the system) can be prevented.